REMARKS

Claims 1, 4-10, 13-17, 20, and 21. Claims 1, 4-10, 13-17 and 20 are presently pending and stand rejected. Claim 21 is added.

Claim 1, 9, and 17 were rejected under 35 U.S.C. 103(a) as being obvious from the combination of Jones in view of Gelsomini. Claim 20 was rejected as being obvious from the combination of Jones, Gelsomini, and Khoury.

Claim 1 recites, among other limitations, "determining if the state of the element is equal to an expected state using a verify circuit, wherein the state of the element is a state of the electrical resistance of the element".

In the Office Action of 2/11/08, Examiner has indicated that Jones discloses "determining if the state of the element is equal to an expected state (VERIFY DATA 0 in Fig. 3b) using a verify circuit (308 in Fig. 3a); and outputting a valid signal (FAST VERIFY OUTPUT of 390 in Fig. 3b) if the state of the element is equal to said expected state (if DR0 is equal to VERIFY DATA 0 in Fig. 3b;". Examiner has also indicated that Gelsomini teaches "a thin oxide gated fuse … wherein a state of the fuse is a state of the electrical resistance of the fuse (inherent as a fuse)." Examiner also indicated that "It would be obvious at the time the invention was made … to substitute a thin oxide gated fuse … as an equivalent memory element … such that the state of the element is a state of the electrical resistance of the element".

In the present office action, Examiner also states "the state of a fuse is inherently determined by its electrical resistance (including the logic state of a high resistance state and a low resistance state). Office Action at 10-11.

Assignee respectfully submits however, that even if the foregoing is true, the combination of Jones and Gelsomini does not teach "determining if the state of the element is equal to an expected state using a verify circuit, wherein the state of the element is a state of the electrical resistance of the element". This is because in the proposed combination, "a thin oxide gated fuse having an oxide less than 2.5 nm think" is substituted for "the memory element of Jones". However, structure 308, which Examiner has indicated that the "verify circuit" which is used for "determining if the state of the element (DR0 in Fig. 3b) is equal to an expected state (VERIFY DATA 0 in Fig. 3b) are (further illustrated in Figure 3b) XOR gates. While XOR gates measure signals –

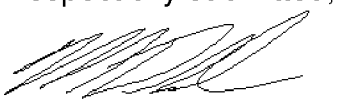
the XOR gates do not electrical resistance. Accordingly, the combination proposed by Examiner does not teach the foregoing limitation, and furthermore is inoperable.

For the reasons above, Assignee respectfully submit that the combination of Jones, and Gelsomini do not teach or fairly suggest "wherein the state is a state of electrical resistance". Accordingly, Examiner is requested to withdraw the rejection to claims 1, 9, 17, and 20 as well as to dependent claims 4-8, 10, and 13-16.

Additionally, claim 21 is added reciting, among other limitations, "wherein the verify circuit comprises a current amplifier". Clearly, 308 in Fig. 3a of Jones, which Examiner alleges is a verify circuit, does not comprises "a current amplifier".

For at least the foregoing reasons, each of the pending claims are in a condition for allowance. Please charge any required fees not paid herewith or credit any overpayment to the Deposit Account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.In view of the foregoing, it is respectfully submitted that the pending claims define allowable subject matter. Should anything remain in order to place the present application in condition for allowance, the Examiner is kindly invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,



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